REMARKS

Summary Of Office Action

Claims 1-41 and 43-53 are pending in this application.

Claims 1-3, 9, 13-15, 21, 25, 26, 29, 31, 32, 38, 43-45 and 51 are finally rejected under 35 U.S.C. § 103(a) as being obvious from Stevens et al. U.S. Patent No. 6,226,729 (hereinafter "Stevens") in view of Ikeda U.S. Patent No. 6,487,086 (hereinafter "Ikeda") in further view of Hartwell U.S. Patent No. 6,724,850 (hereinafter "Hartwell").

Claims 4, 5, 7, 8, 10-12, 16, 17, 19, 20, 22-24, 27, 28, 30, 33, 34, 36, 37, 39-41, 46, 47, 49, 50, 52 and 53 are finally rejected under 35 U.S.C. § 103(a) as being obvious from Stevens, Ikeda, and Hartwell in further view of Johnson et al. U.S. Patent No. 5,577,236 (hereinafter "Johnson").

Claims 6, 18, 35, and 48 are finally rejected under 35 U.S.C. § 103(a) as being obvious from Stevens, Ikeda, and Hartwell in further view of Olarig et al. U.S. Patent No. 6,134,638 (hereinafter "Olarig").

The Examiner's final rejection is respectfully traversed.

Applicant's Reply to the 35 U.S.C. § 103(a) Rejections

I. Rejection of Independent Claims 1, 9, 13, 21, 25, 26, 29, 31, 38, 43, and 51

Independent claims 11, 9, 13, 21, 25, 26, 29, 31, 38, 43, and 51 are, at least in part, directed toward methods, memory controllers, and apparatus for selecting an operating speed of a memory module interface. The number of memory modules is counted and a running tally of the number of memory modules is maintained based on the counting. Multiple clock

signals are simultaneously generated at different frequencies to provide a selectable operating speed for the memory module interface. The maximum speed at which all of the memory module can operate is determined. A look-up table containing a plurality of memory clock frequencies each associated with a number and a type of memory modules is accessed. Based on comparing a final tally of the number of memory modules with the look-up table, only one of the multiple clock signals is selected to provide the operating speed of the memory module interface, where the operating speed is slower than the determined maximum speed. The selected clock signal is then provided to all of the memory modules.

The Examiner's position in this rejection appears to be that (1) Stevens shows all of the features all applicant's independent claims except, (a) simultaneously generating multiple clock signals at different frequencies and (b) selecting an operating speed to be slower than the determined maximum speed by comparing a final tally of the number of memory modules with a look-up table, (2) Hartwell compensates for the first deficiency in Stevens by simultaneously generating multiple clock signals at different frequencies, (3) Ikeda compensates for the second deficiency in Stevens by selecting an operating speed to be slower than the determined maximum speed based on a final tally of the number of memory modules, and (4) even though Ikeda does not show using a look-up table to select the operating speed based on the number of memory modules that both Harwell and Stevens show tables to organize data and therefore the use of a look-up table in this manner would be obvious. Applicant respectfully disagrees with the Examiner's position.

None of these references, taken alone or in combination, show or suggest "accessing a look-up table containing a plurality of memory clock frequencies each associated with a number and a type of memory modules" and selecting a clock signal "based on at least comparing a final tally of the number of said memory modules with the look-up table," as recited by applicant's independent claims.

The Examiner admits that this feature of applicant's independent claims is not show by Ikeda. However the Examiner contends that "Hartwell and Stevens both teach the well known concept of using a look-up table to organize associations between elements." Based on this supposed teaching of Hartwell and Stevens, the Examiner concludes that it would have been obvious to use the look-up tables of Hartwell and Stevens in order to select a clock signal based on a final tally of the number of memory modules. However, Hartwell and Stevens do not use look-up tables in this manner.

In fact, the tables of Hartwell and Stevens are not look-up tables and do not make up for the deficiency in Ikeda. Table 1 of Hartwell lists examples of slow clock speeds that can be generated from faster clock speeds based on programmable divisor settings. This is not a look-up table. Rather, this table of Hartwell merely illustrates different configurations in which the system can be configured to operate. Similarly, tables 1-4 of Stevens are also not look-up tables. Tables 1-4 of Stevens refer to the type and form of data registers, operands, and variables used by the system of Stevens. For example, table 1 of Stevens describes the content of each of the sixteen bits of a device register data register. Thus, the tables of Stevens and Hartwell are not look-up tables used by

their respective systems to select, for example, an operating speed. Instead these tables are merely representations of information used to help describe the manner in which their various components operate.

Accordingly, for at least this reason, applicant respectfully submits that neither Stevens nor Ikeda nor Hartwell shows or suggests selecting a clock signal based on comparing a final tally of the number of said memory modules with a look-up table as recited by applicant's independent claims. Whether or not the combination of these references are proper, the combination of features which these references cumulatively contribute also falls short of showing or suggesting applicant's claimed

For at least this reasons applicant respectfully requests that the rejection of independent claims 1, 9, 13, 21, 25, 26, 29, 31, 38, 43, and 51 under 35 U.S.C. § 103(a) as being obvious from Stevens, Ikeda, and Hartwell be withdrawn.

II. Rejection of Independent Claims 11, 12, 23, 24, 30, 40, 41, 52, and 53

Applicant respectfully submits that amended independent claims 11, 12, 23, 24, 30, 40, 41, 52, and 53 are allowable for at least the same reasons as amended independent claims 1, 9, 13, 21, 25, 26, 29, 31, 38, 43, and 51. Thus, neither Stevens nor Ikeda nor Hartwell nor Johnson shows or suggests all of the elements of applicant's amended independent claims. Whether or not the combination of these references are proper, the combination of features which these references cumulatively contribute also falls short of showing or suggesting applicant's claims. For at least this reasons applicant respectfully requests that the rejection of

independent claims 11, 12, 23, 24, 30, 40, 41, 52, and 53 under 35 U.S.C. § 103(a) as being obvious from Stevens, Ikeda, Hartwell, and Johnson be withdrawn.

II. Rejection of Dependent Claims

For at least the reasons discussed above with respect to applicant's amended independent claims, dependent claims 2-8, 10, 14-20, 22, 27, 28, 32-37, 39, and 44-50, which depend directly or indirectly from claims 1, 9, 11-13, 21, 23-26, 29-31, 38, 40, 41, 43, and 51-53 are also not rendered obvious from the various combinations of Stevens, Ikeda, Hartwell, Johnson, and Olarig (i.e., dependent claims are patentable if their independent claim is patentable). Accordingly, applicant respectfully requests that the rejections of dependent claims 2-8, 10, 14-20, 22, 27, 28, 32-37, 39, and 44-50 be withdrawn.

Conclusion

The foregoing demonstrates that claims 1-41 and 43-53 are patentable. This application is therefore in condition for allowance. Reconsideration and allowance are accordingly respectfully requested.

Respectfully submitted,

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